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(71) Applicant
Quick Turnaround Logic Limited

(Incorporated in United Kingdom)

Unit 4, Heron Industrial Estate, Spencers Wood, Reading, Berkshire RG7 1PG

(72) Inventor
Richard Kent Percival

(74) Agent and/or Address for Service
Urquhart-Dykes & Lord,
47 Marylebone Lane, London W1M 6DL

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H1K
Selected US specifications from IPC sub-class H01L

(54) **Tape automatic bonding or circuitry to an electrical component**

(57) A method of tape automatic bonding circuitry to an electrically conductive or responsive component, preferably an integrated circuit, is described which method comprises:
(a) preparing the component 10 with connection points;
(b) preparing a tape with inner leads 12 lying in one plane to correspond to the connection points;
(c) attaching the inner leads to the connection points to form inner lead bonds;
(d) excising the bonded component from the tape to provide a tape carrier support ring with outer leads 16;
(e) aligning the tape carrier support ring into a substrate having circuitry corresponding to the said outer leads and an opening corresponding to the shape and size of the support ring; and
(f) attaching the outer leads to circuitry of the substrate.

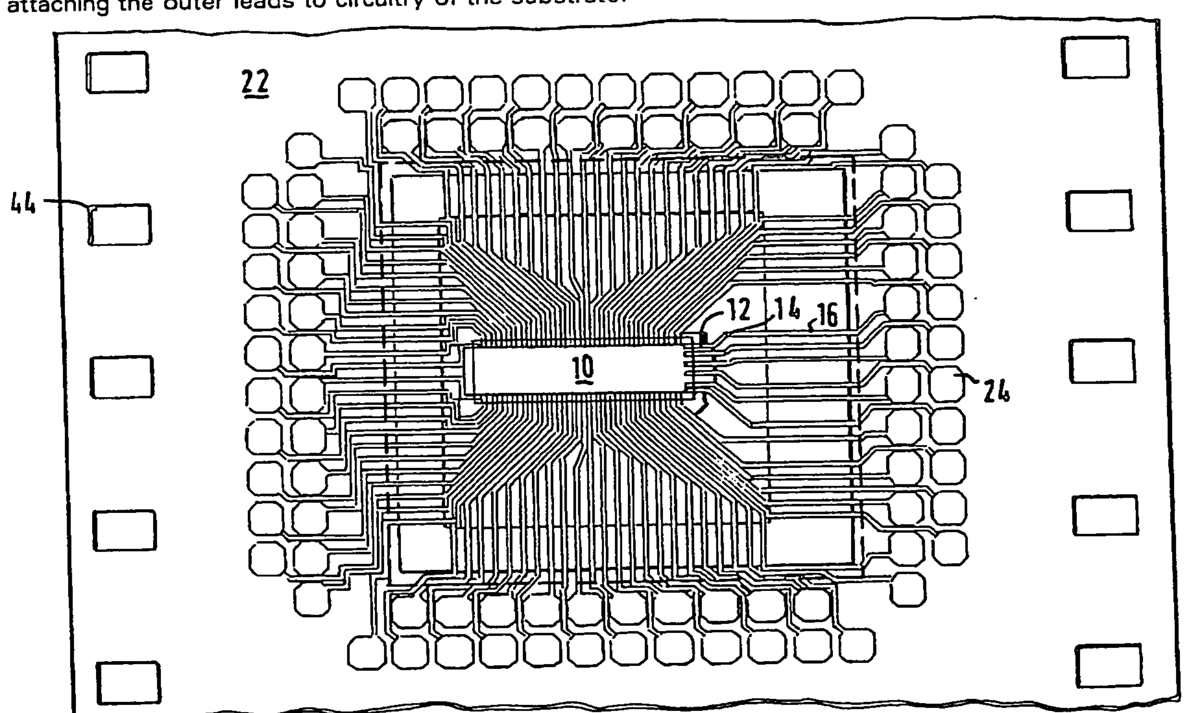

FIG.2b

The drawing(s) originally filed was/were informal and the print here reproduced is taken from a later filed formal copy.

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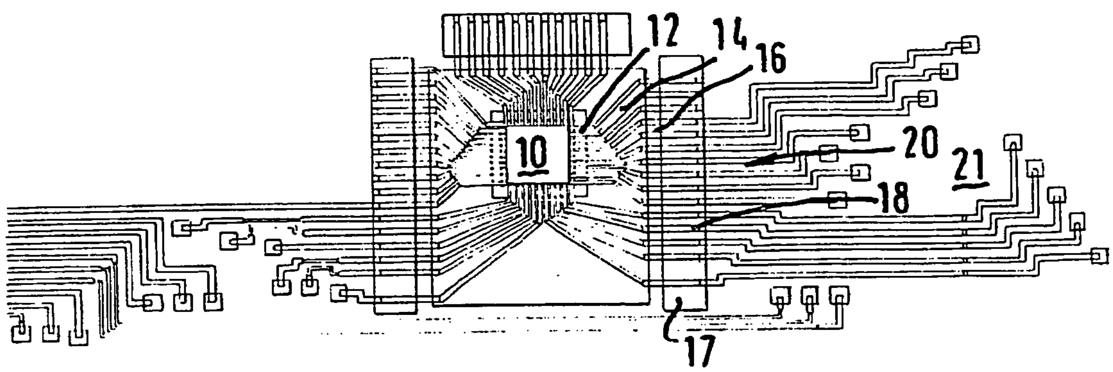
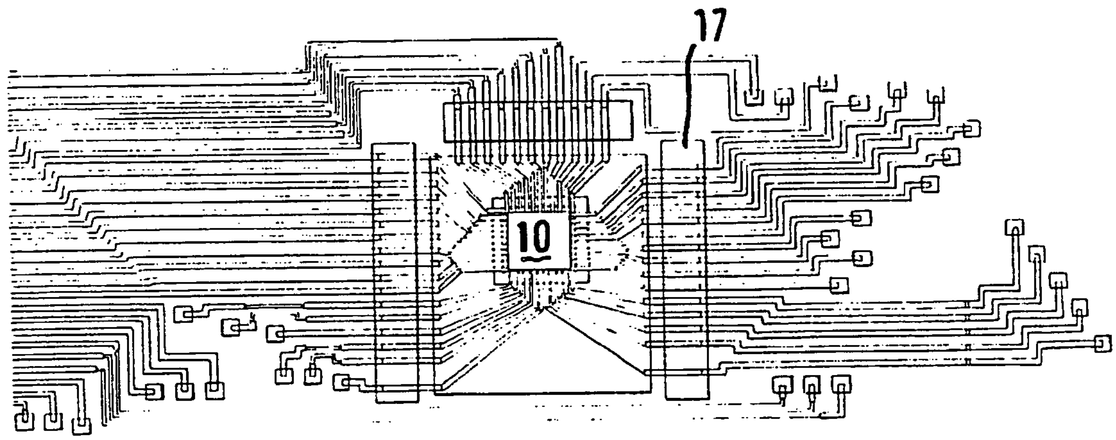
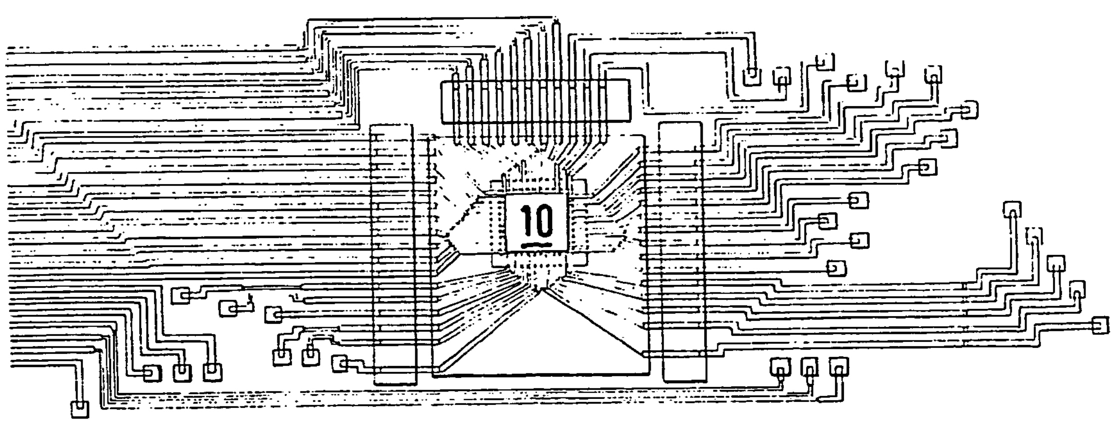
FIG.1







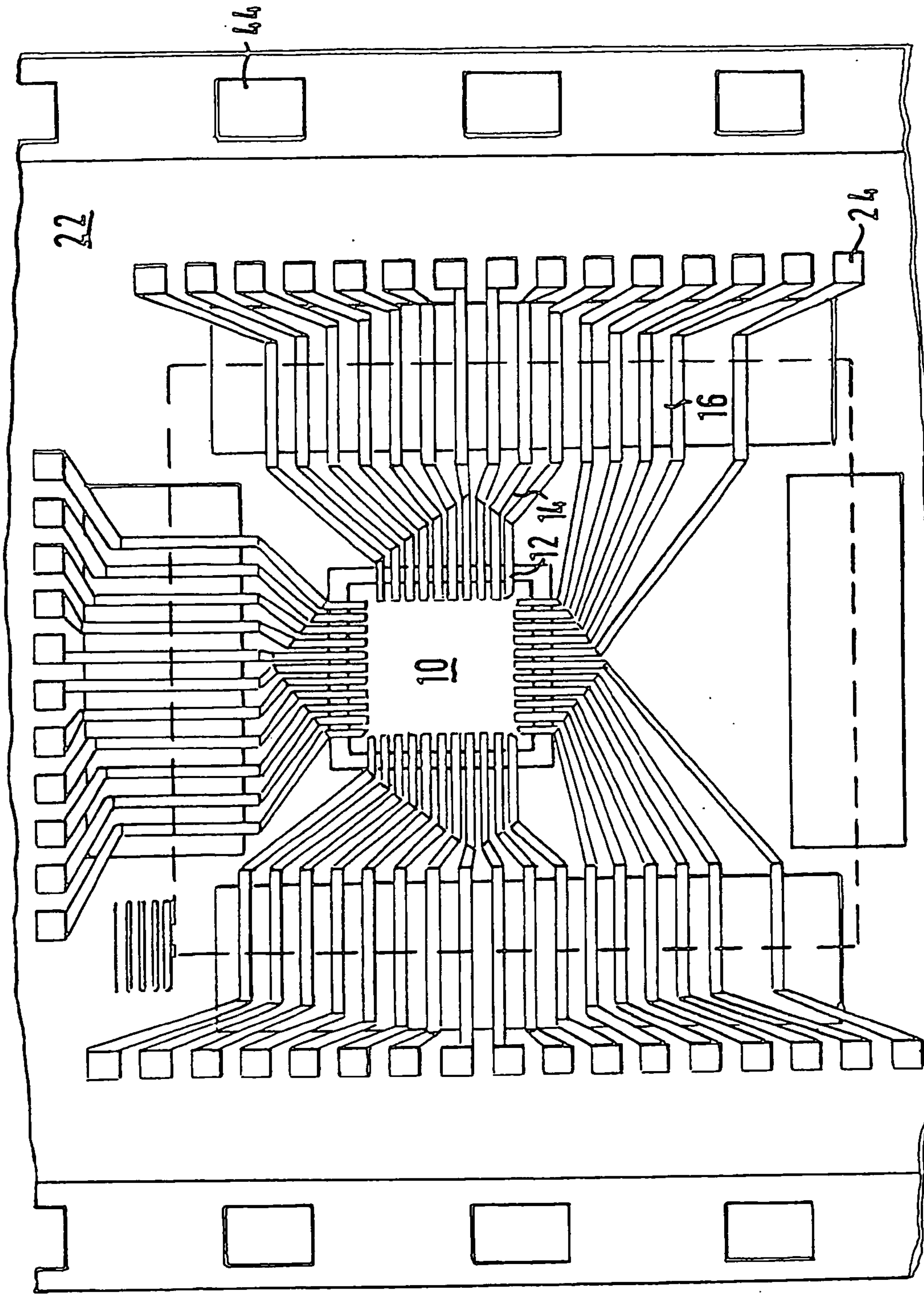


FIG. 2a

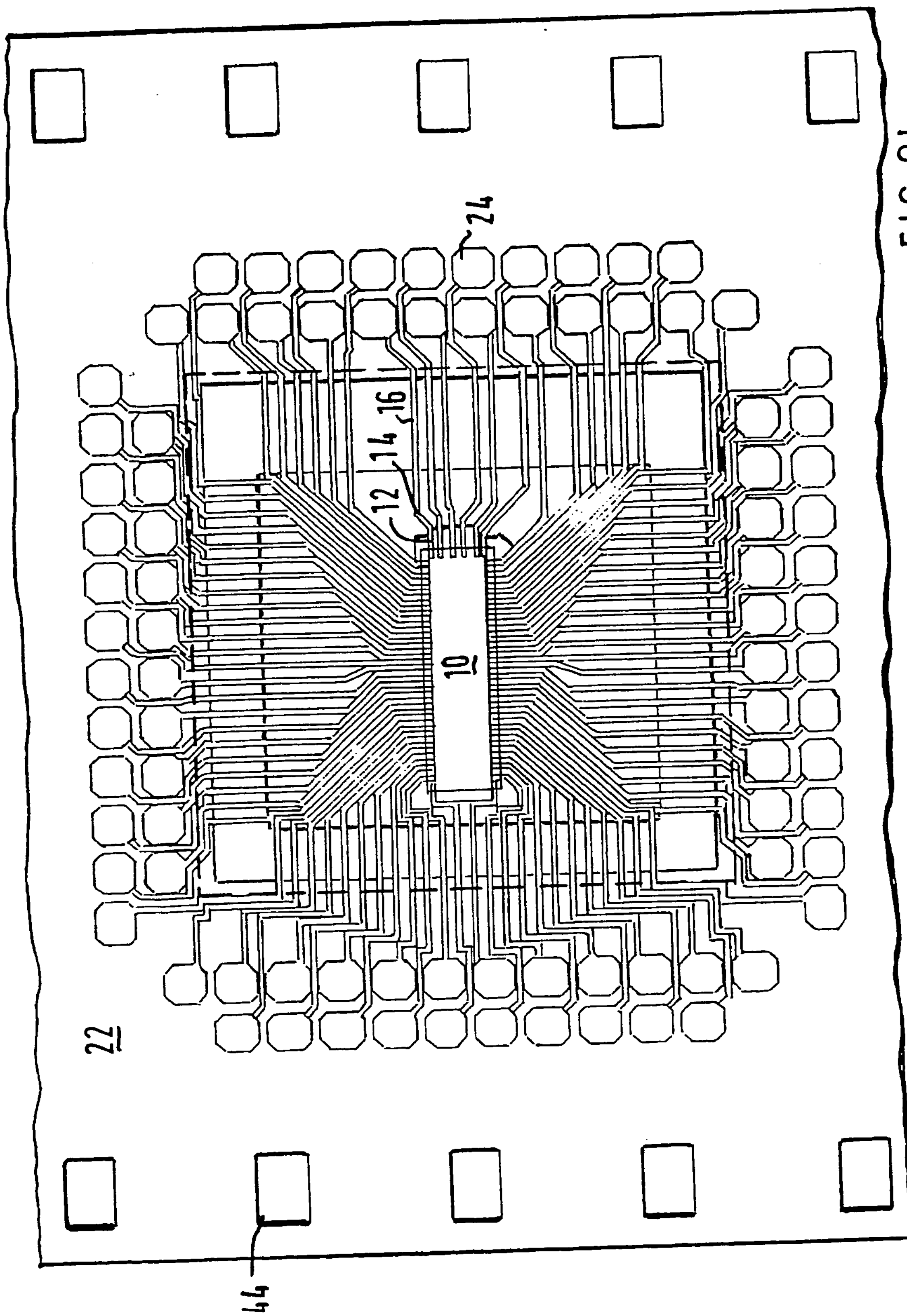


FIG.2b

FIG.3

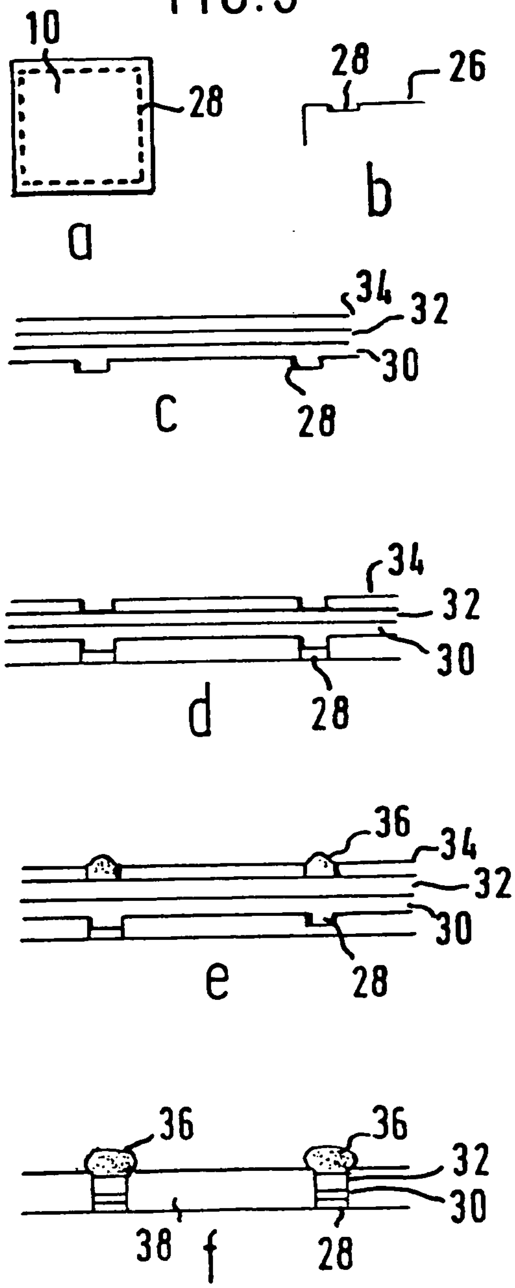

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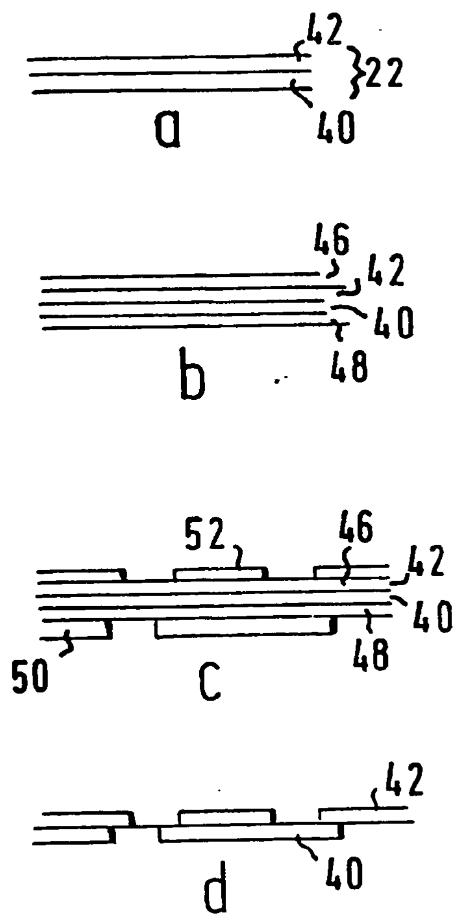
FIG.4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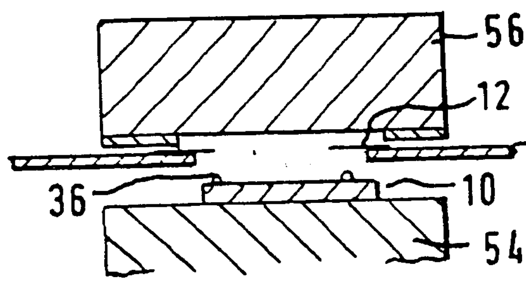

FIG. 5

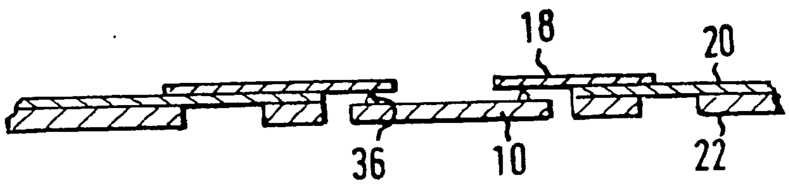

FIG. 6

SPECIFICATION

Tape automatic bonding

The present invention relates to an improved method of tape automatic bonding (TAB).

The standard TAB process, a surface mounting technique, involves mounting integrated circuits on a sprocketed tape with a series of micro-interconnect patterns. The tape material can be copper, or a polymer/metal laminate, with the micro-interconnects etched out of the copper or metal. When an integrated circuit is attached to a substrate in this manner, it occupies the same or only slightly more substrate area as a wire bonded chip, thus providing the ability to pack the chips densely.

Various tape automatic bonding techniques are well known in the art and are for example described in U.S. Patent No. 4064552—Angelucci et al. A useful review of TAB techniques can be found in Electronics dated 18th December 1980. This article discusses TAB techniques, both in the face-down format as well as the face-up format. A further discussion of TAB by D.J. Small can be found in Circuit World Volume 10, No. 3, 1984.

One of the major disadvantages of the present TAB techniques is that the tape carrier once excised from the tape presents cantilevered ends which must be accurately placed over the leads of the circuitry into which it is to be mounted. The cantilevered leads are very delicate and extremely difficult to maintain in their relative positions and as such can be easily deformed. After the chip in its tape carrier has been excised from the tape, individual mechanical alignment is required and individual connection of each of the leads may be necessary to ensure proper connection to the final circuitry.

The present invention attempts to overcome these disadvantages by providing an improved tape automatic bonding technique of electrically conductive or responsive components, particularly integrated circuits although other circuitry can be dealt with in the same way e.g. LEDs, LCDs etc., whereby:

(1) the leads of the tape carrier are produced from an integrated circuit data base,

(2) the outer leads of the tape carrier and leads contained on the final circuitry are produced from the same mechanical artwork,

(3) cantilevered connections are eliminated,

(4) an opening is provided in the circuitry into which the excised tape is to be installed.

The present invention provides a method of tape automatic bonding circuitry to an electrically conductive or responsive component which method comprises:

(a) preparing the component with connection points;

(b) preparing a tape with inner leads lying in one plane, said leads lying in one plane to correspond to the connection points;

(c) attaching the inner leads to the connection points to form inner lead bonds;

(d) excising the bonded component from the tape to provide a tape carrier support ring with outer leads;

(e) aligning the tape carrier support ring into a substrate having circuitry corresponding to the said outer leads and an opening corresponding to the shape and size of the support ring; and

(f) attaching the outer leads to circuitry of the substrate.

The component is preferably an integrated circuit although it may be any other electronic component such as LED, LCD, etc. Connection points may be bump connections on the surface of the component or merely electrically conductive points to which conductive traces or leads may be connected. In this case, the bump connections may be applied to the inner leads for connection to the electrically conductive points.

In particular, in a preferred embodiment, the present invention provides a method of tape automatic bonding an integrated circuit into an associated substrate, which method comprises:

(a) preparing an integrated circuit with bump connections;

(b) preparing a tape with inner leads lying in one plane, said leads lying in one plane to correspond to the bump connections;

(c) attaching the inner leads to the bump connections to form inner lead bonds;

(d) excising the bonded integrated circuit from the tape to provide a tape carrier support ring with outer leads;

(e) aligning the tape carrier support ring into a substrate having circuitry corresponding to the said outer leads and an opening corresponding to the shape and size of the support ring; and

(f) attaching the outer leads to circuitry of the substrate.

It is preferred that the tape is a metal tape coated with an insulating material, preferably a plastic coated metal tape and more particularly a copper polyimide tape.

In one embodiment the tape with inner leads is prepared by coating the tape with a photo-resist, imaging the resist using a mask with the desired metallic pattern, developing the resist to expose the metal to be removed and etching the metal to leave the desired pattern, including the provision of inner leads for connection to the integrated circuit. Eletroless tin may be applied to the copper of the tape and the inner leads may be mass bonded to the integrated cicuit.

Although an etching technique for preparing the conductive traces on tape is described, other techniques may also be used. For example, the conductive traces may be applied by an additive technique.

The component or integrated circuit is preferably tested in situ after attaching the inner leads to the connection points or bump connections.

The outer leads are preferably mass bonded to the circuitry of the substrate to complete the final connection of the component or integrated circuit. The mass bonding is preferably by a reflowing technique.

The present invention will be further described by way of example only (wherein the electrically conductive or responsive component is preferably an integrated circuit), with reference to the accompanying drawings, in which:

Figure 1 shows an integrated circuit in position with its final circuitry;

Figures 2a and 2b show alternative forms of a tape with inner leads bonded to and holding an integrated circuit in position;

Figures 3a to 3f are a series of diagrams showing preparation of bumped integrated circuits;

Figures 4a to 4d are a series of diagrams showing preparing of tape;

Figure 5 shows the connection of the integrated circuit to the tape; and

Figure 6 shows in cross-section an integrated circuit in position in the substrate circuit.

Referring to Figure 1, this figure shows the complete circuitry including the integrated circuit or chip 10 included into the circuitry to which it relates and in which it is to be used. The integrated circuit 10 having inner leads 12 are connected via an expansion network of leads 14 to copper outer leads 16. Between the expansion network leads 14 and copper outer leads is an outer lead bonding slot 17. The outer leads are connected to the leads 18 of the circuitry generally designated 20 to which the integrated circuit 10 is to be attached within a circuitry substate 21. Figures 2a and 2b show the integrated circuit 10 enclosed within a tape from which the integrated circuit 10 will be excised prior to placing in its final circuitry. As shown in Figures 2a and 2b, the inner and outer leads 12 and 16 are copper preferably etched from a polyimide copper. The outer leads 16 extend to test sites 24 enabling the integrated circuit 10 to be tested before it is removed from the tape.

The techniques of tape automatic bonding of the present invention will be further described by reference to a series of figures beginning with Figure 3.

Referring to Figures 3a and 3b, the integrated circuit is in the form of a chip 10 having an inert upper layer 26, e.g. plastic coated or glassy, with openings 28 for connections to bonds to enable the chip to be incorporated into further circuitry. The bond connection openings 28 expose metal, preferably aluminium with a small amount of silicon. The inert upper surface with aluminium exposed through openings is subsequently vacuum coated with a thin film of, for example, titanium 30 and then tungsten 32 (see Figure 3c). These metals are generally chosen because there is no inter-metallic action with aluminium. However it is possible to use other metals as required. A photoresist 34 layer can be applied to the top surface of the tungsten layer. The bump areas are imaged as shown in Figure 3d such that the photo-resist is removed from the area above the aluminium opening 28. A gold bump 36 is formed in this opening or window preferably by means of electroplating in a bath using the titanium tungston layer as the cathodic connection. The gold builds up on the tungsten in the areas where the resist is missing as shown in Figure 3e. Following the deposition of the gold film to form the bumps, the remaining photo-resist is removed and finally the tungsten and titanium overlayer between the gold bumps is etched away to leave the formation as shown in Figure 3f of an aluminium 28, titanium 30, tungsten 32 and gold terminal 36. The result is a gold rivet attached to the chip via tungsten titanium and an aluminium platform embedded in an inert passivating coating such as glass.

As shown in Figure 4, a tape in the form of conventionally sized film tape, such as 16 mm or 35 mm, although other sizes can be used if required, is used as the carrier tape. The tape is generally in the form of a copper-clad 40-35 mm polyimide tape 42 with the conventional sprocket holes 44 punched in the polyimide in a similar manner to those on standard film. To prepare the tape, a rolled annealed copper foil 40, generally of a thickness of about 35 um and 25 mm wide is attached to one side of the tape either directly or by means of acrylic adhesive. The copper polyimide tape may be a Kapton (R.T.M.) tape produced by Minnesota Mining and Manufacturing Company. Alternatively the tape may be any multilayer metal plastic tape of the polyester or polyimide type coated with copper or aluminium.

The tape 22 is subsequently coated with a photo-resist 46,48 on both sides and using a metal mask 50,52 showing the desired pattern is exposed on both sides. The photoresist is removed by developing, and the undesired metal is etched away using for example ferrous chloride. Then the polyimide is etched away using organic solvents leaving the outer and inner leads clear of the plastic with an isolated polyimide ring connected to the remainder of the film via outer leads. The mask used in the photo-resist technique is drawn with a specific circuit design suitable for the chip to be connected within the tape.

Electroless tin may be applied to the copper of the tape, then gold bumped chips may be attached to the tape using a heated tool so that the chip with its gold bumps and the

electroless tin of the tape are heated to a temperature sufficient to allow a eutectic alloying of the tin with the gold but not at a temperature to allow melting. The integrated circuit 10 is generally prepared in the form of a wafer. The wafer is cut or sawn and expanded slightly. The integrated circuit 10 is removed from the wafer by means of an automatic arm and placed onto an anvil or a counter thermode 54. The prepared tape or film 22 is run on sprockets a short distance from a counter thermode 54 and is placed in position, aligned using a television camera or by means of manual alignment or by optical pattern techniques. The anvil rises, the thermode 56 is applied and the inner leads are connected to the gold bumps in a mass bonding technique. The tape 22 is advanced with the chip in position and can be tested. Once the testing has taken place via test sites 24 and the integrated circuit has been found to be satisfactory, the integrated circuit is removed from the carrier tape 22 by cutting the inside of the outer expansion zone and excising the outer leads along with a protective outer polyimide ring, so that the chip and carrier are suspended wthin a protective polyimide ring connected by the outer leads. The excised areas are shown with the dashed line in Figures 2a and 2b.

A circuitry substrate 21 generally but not exclusively in the form of a film can also be prepared with its circuitry using exactly the same circuitry design as for the tape preparation, allowing the integrated circuit to be positioned by manual, optical or pattern techniques or by use of a television camera. The outer bonding leads are connected to the leads of the circuit by means of a thermode in a manner similar to that shown in Figure 5 for the connection of the inner leads to the integrated circuit. The circuitry substrate 21 may be a flexible film or can be a rigid material. In addition, the matching circuitry may be designed to accomodate one or a number of tape mounted devices 10 as shown in Figure 1.

This technique allows easy connection and alignment of the integrated circuit with the inner leads by visual means. It also allows support in the expansion zone for the outer leads by means of the Kapton (R.T.M.) ring. Finally it allows mating of the outer leads to a similar circuitry which can be positioned by eye and subsequently be bonded to that circuitry.

The substrate 22, e.g. the polyimide copper tape, which may be either the two-layer tape, or copper on polyimide bonded with adhesive as a three-layer tape, is generally thin and is generallly of the same thickness as the integrated circuit such that the integrated circuit, once bonded to the tape, does not provide any greater thickness than the tape.

The present invention has significant advantages over the prior art, in that the chip contained within the polyimide copper tape is substantially the same thickness as the film and avoids the problem of the chip being above or below the substrate surface. The connecting inner and outer leads are substantially planar. Thus, no account need be taken of the geometrical distortion of expansion leads to provide cantilevered support for the integrated circuit.

A further advantage of the present invention is that cantileverd connections can be eliminated by the use of an annular protective ring surrounding the outer leads as shown in Figures 2a and 2b.

In addition, chips can be mounted face-up. Thus, the same design of connection circuitry can be used in preparing the insertion of the integrated circuit within the polyimide copper tape and also be used in preparing the circuitry to which the outer leads are to be connected.

Alternatively, the chip can be mounted face down. Thus the ciciutry associated with the chip, i.e. the inner and outer leads, is mounted on the opposite side of the tape carrier support to the circuitry into which the chip is being mounted.

Another advantage of the present invention is that an opening is provided in the circuitry into which the excised tape carrier is to be installed. The opening can be of the same precise shape and size of the support ring of the tape carrier and is preferably drawn from the same design database. Thus alignment problems can be overcome. When the excised tape carrier support ring is placed in the substrate prior to final connection, because of the closely matching nature of the two items alignment can carried out by eye or by less sophisticated techniques than have been possible heretofore.

CLAIMS

1. A method of tape automatic bonding circuitry to an electrically conductive or responsive component which method comprises:

(a) preparing the component with connection points;

(b) preparing a tape with inner leads lying in one plane, said leads lying in one plane to correspond to the connection points;

(c) attaching the inner leads to the bump connection points to form inner lead bonds;

(d) excising the bonded component from the tape to provide a tape carrier support ring with outer leads;

(e) aligning the tape carrier support ring into a substrate having circuitry corresponding to the said outer leads and an opening corresponding to the shape and size of the support ring; and

(f) attaching the outer leads to circuitry of the substrate.

2. A method as claimed in claim 1 wherein the component is an integrated circuit.

3. A method of tape automatic bonding an integrated circuit into an associated subsrate, which method comprises:

(a) preparing an integrated circuit with bump connections;

(b) preparing a tape with inner leads lying in one plane, said leads lying in one plane to correspond to the bump connections;

(c) attaching the inner leads to the bump connections to form inner lead bonds;

(d) excising the bonded integrated circuit from the tape to provide a tape carrier support ring with outer leads;

(e) aligning the tape carrier support ring into a substrate having circuitry corresponding to the said outer leads and an opening corresponding to the shape and size of the support ring; and

(f) attaching the outer leads to circuitry of the substrate.

4. A method as claimed in claim 1 or claim 3 wherein the tape is copper polyimide tape.

5. A method as claimed in claim 4 wherein the tape with inner leads is prepared by coating the tape with a photoresist, covering the photo-resist with a metal mask showing the desired circuitry, developing the photo-resist to expose unwanted metal, and etching away said unwanted metal to leave the desired circuitry to provide inner leads for connection to the integrated circuit.

6. A method as claimed in claim 5 wherein eletroless tin is applied to the copper of the tape and the inner leads are mass bonded to the integrated cicuit.

7. A method as claimed in any one of the preceding claims wherein the component or integrated circuit is tested in situ after attaching the inner leads to the connection points or bump connections.

8. A method as claimed in any one of the preceding claims wherein the outer leads are mass bonded to the circuitry of the substrate.

9. A method as claimed in any one of the preceding claims wherein the bonded component or integrated circuit is excised from the tape to provide a tape carrier support ring having an outer protective ring.

10. A method as claimed in claim 1 substantially as hereinbefore described with reference to and as illustrated in the accompanying drawings.

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